IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Matthew J. Adiletta	Art Unit	: Unknown
Serial No.	: Unknown	Examiner	: Unknown
Filed	: Herewith		
Title	: PARALLEL PROCESSOR ARCHITECTURE		

MAIL STOP PATENT APPLICATION
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Under 35 USC §120, this application relies on the earlier filing date of application serial number 09/387,111, filed on August 31, 1999. The references were submitted to and/or cited by the Office in the prior application and, therefore, are not provided in this application.

This statement is being filed with the application. Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 7-8-03

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July 8, 2003
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Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-075002	Application No.
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Matthew J. Adiletta, et al.	
		Filing Date Not Yet Assigned	Group Art Unit

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	6,272,616	08/07/2001	Fernando et al.	712	228	
	AB	6,079,008	06/20/2000	Clery, III	712	11	
	AC	6,023,742	02/08/2000	Ebeling et al.	712	17	
	AD	5,915,123	06/22/1999	Mirsky et al.	712	16	
	AE	4,745,544	05/17/1988	Renner et al.	712	11	
	AF	4,514,807	04/30/1985	Nogi	712	21	
	AG	3,940,745	02/24/1976	Sajeva	340	172.5	
	AH	3,792,41	02/12/1974	Wymore et al.	712	248	
	AI	3,478,322	11/11/1969	Evans	712	248	
	AJ						

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	AK	WO 94/15287	07.07.94	PCT				
	AL	WO 97/38372	16.10.97	PCT				
	AM							
	AN							
	AO							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	AP	"Multithreaded Processor Architectures", IEEE Spectrum, 32(1995) August No. 8, New York, US, pp. 38-46.
	AQ	**M. Tremblay *et al.***, "A Three Dimensional Register File for Superscalar Processors," IEEE Proceedings of the 28th Annual Hawaii Int'l Conference on Sysems Sciences, 1995, pp. 191-201.
	AR	**M.R. Thistle *et al.***, "A Processor Architecture For Horizon," IEEE 1998, pp. 35-41.
	AS	**M. Fillo *et al.***, "The M-Machine Multicomputer," IEEE Proceedings of MICrO-28, 1995, pp. 146-156.
	AT	**T. Litch *et al.***, "StrongARMing Portable Communications," IEEE Micro 1998, pp. 48-55.
	AU	**M. Wazlowski *et al.***, "PRISM-II compiler and architectgure, IEEE Proceedings, Workshop on FPGAs for Custom Computing Machines," 1993, IEEE.

Examiner Signature	Date Considered

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
	AV	**S. Trimberger *et al.***, "A Time-Multiplexed FPGA," Proceedings of the 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 1997, IEEE.
	AW	**G. Haug *et al.***, "Reconfigurable Hardware as Shared Resource for Parallel Threads," IEEE Symposium on FPGAs for Custom Computing Machines, 1998, IEEE.
	AX	**J.R. Hauser *et al.***, "a MIPS Processor with a reconfigurable Coprocessor, Proceedings of the 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 1997, IEEE.

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